

REMARKS

Claims 6-9 and 11-19 are pending in the present application. Replacement claims 6, 11 and 16 are presented herewith.

Drawings

The drawings have been objected to under 37 C.F.R. 1.83(a) as allegedly failing to show every feature of the invention specified in the claims. The Examiner has required that the insulating layer, contact hole and connecting wire be shown in the drawings, or the corresponding features must be canceled from the claims.

Proposed Fig. 1(i) has been submitted in a Letter Submitting Drawing Figure filed concurrently herewith. As illustrated in proposed Fig. 1(i), insulating layer 50, contact holes 52 and aluminum wiring 54 are depicted, as supported on page 13, lines 12-17 of the application. The Examiner is respectfully requested to approve entry of proposed Fig. 1(i) and to withdraw the objection to the drawings. Formal Fig. 1(i) will be prepared and filed upon approval by the Examiner and subsequent indication of allowance of the present application.

Claim Rejections-35 U.S.C. 102

Claims 6-9 and 11-19 have been rejected under 35 U.S.C. 102(b) as being clearly anticipated by the Yoo et al. reference (U.S. Patent No. 5,605,853). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the

following reasons.

The semiconductor device of claim 6 includes in combination a field oxide "formed on the substrate between said first and second gates", and a protective layer "formed on said field oxide to prevent overetching of said field oxide, said protective layer being a material different than said field oxide". Applicant respectfully submits that the Yoo et al. reference does not disclose these features.

The Examiner has asserted that layer 21 in any of Fig(s). 2-7 of the Yoo et al. reference may be interpreted as the protective layer of claim 6. The Examiner has apparently taken this position because layer 12 **appears** to be disposed on field oxide film (FOX) 12, in Fig. 2 for example. However, as described in column 4, lines 2-4 of the Yoo et al. reference, layer 21 is a floating gate for a floating gate memory cell (for an EEPROM). Typically, floating gates exchange charges with a diffusion layer formed in the surface of a semiconductor substrate. The floating gate is thus typically formed on a thin insulating layer, such as a tunnel oxide layer, so that exchange of charges between the diffusion layer may occur. Accordingly, for layer 21 of the Yoo et al. reference to be a floating gate as described in the reference, it should reasonably be assumed that layer 21 would be formed on a thin insulating layer over a diffusion layer, such as **behind** FOX layer 12, not thereon. [Applicant emphasizes that floating gate 21 is not specifically described as formed on FOX layer 21.]

Applicant also respectfully emphasizes that floating gate 21 of the Yoo et al. reference is not described or even remotely suggested as a protective layer formed on

a field oxide, to prevent overetching of the field oxide, as featured in claim 6. In other words, even assuming that layer 21 is formed on FOX layer 12 (which Applicant does not concede), there is no suggestion or description that layer 21 is provided at a point during processing to prevent overetching. Accordingly, Applicant respectfully submits that the semiconductor device of claim 6 distinguishes over the Yoo et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 6-9, is improper for at least these reasons.

Applicant also respectfully submits that claims 11 and 16 distinguish over the Yoo et al. reference as relied upon by the Examiner for at least somewhat similar reasons. Particularly, each of independent claims 11 and 16 respectively include in combination a protective layer "formed on said field oxide to prevent overetching of said field oxide, said protective layer being a material different than said field oxide". As emphasized previously, it is not clear how floating gate layer 21 of the Yoo et al. reference can be formed on FOX layer 12. Also, layer 21 of the Yoo et al. reference is not disclosed or even remotely suggested as being a protective layer formed on a field oxide to prevent overetching of the field oxide, as featured in the above noted claims. Accordingly, Applicant respectfully submits that claims 11 and 16 distinguish over the Yoo et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 11-19, is improper for at least these reasons.

Conclusion

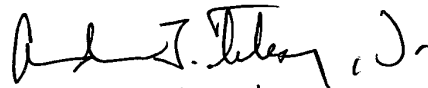
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

AJT:dmc

VOLENTINE FRANCOS, P.L.L.C.
12200 Sunrise Valley Drive, Suite 150
Reston, Virginia 20191
Telephone No.: (703) 715-0870
Facsimile No.: (703) 715-0877

Enclosures: Version with Marked-Up Changes



Serial No. 09/768,271
RECEIVED

VERSION WITH MARKED-UP CHANGES

NOV -4 2002

TECHNOLOGY CENTER 2800

Additions/Deletions to the Specification:

Page 13, lines 12-17:

Thereafter, the side-wall 37 is formed by implementing the anisotropic etching such as the RIE with respect to the oxide layer 36 (FIG. 1(h)). Then, the insulating layer 50 and the contact [hole] holes 52 are formed, and the aluminum wiring 54 is conducted by the normal processes, thus completing the MOSFET (FIG. 1(i)).

Additions/Deletions to the Claims:

6. (Three Times Amended) A semiconductor device comprising :

first and second gates formed on active regions of a substrate, said first and second gates each consisting of a refractory metal layer on a polysilicon layer;

a field oxide formed on the substrate between said first and second gates;

side walls formed on side surfaces of said first and second gates, said side walls being a silicon oxide film;

a protective layer formed on said field oxide to prevent overetching of said field oxide, said protective layer being a material different than said field oxide;

an insulating layer formed on the substrate, said first and second gates, said side walls, said field oxide and said protective layer;

[a] contact [hole] holes formed through said insulating layer; and

a connecting wire coupled to said first and second gates [gate] through said

contact [hole] holes.

11. (Amended) A semiconductor device comprising:

a gate formed on an active region of a substrate;

a field oxide formed on the substrate adjacent the active region;

a protective layer formed on said field oxide to prevent overetching of said field oxide, said protective layer being a material different than said field oxide;

an insulating layer formed on the substrate including said gate, said field oxide and said protective layer;

a contact hole formed through said insulating layer; and

a connecting wire coupled to said gate through said contact hole,

said protective layer being formed on said field oxide only.

16. (Amended) A semiconductor device comprising:

a gate formed on an active region of a substrate, said gate consisting of a refractory metal layer on a polysilicon layer;

side walls formed on side surfaces of said gate, said side walls being a silicon oxide film;

a field oxide formed on the substrate adjacent the active region;

a protective layer formed on said field oxide to prevent overetching of said field oxide, said protective layer being a material different than said field oxide;

an insulating layer formed on the substrate, said gate, said side walls, said field

oxide and said protective layer;

a contact hole formed through said insulating layer; and

a connecting wire coupled to said gate through said contact hole,

said protective layer being formed on said field oxide only.